CLAIMS

What is claimed is:

1. A method of programming a multiple level cell comprising:

applying a gate voltage approximately equal to a desired threshold voltage plus a minimum threshold value;

applying a drain voltage, wherein said drain voltage gradually increases from a first level toward a second level; and

removing said drain voltage, when a drain current decreases.

2. The method according to Claim 1, further comprising removing said gate voltage, when said drain current decreases.

3. The method according to Claim 1, wherein said removing said drain voltage when said drain current decreases is adapted to reduce a distribution of said desired threshold voltage.

4. The method according to Claim 1, wherein said removing said drain voltage when said drain current decreases is adapted to increase a programming reliability of said memory cell.

5. The method according to Claim 1, wherein said multiple level cell is programmed to said desired threshold value when said drain current decreases.

6. A method of programming a memory device comprising:

a) applying a first programming voltage to one of a plurality of wordlines corresponding to a cell to be programmed, wherein said first programming voltage corresponds to a desired threshold voltage;

b) applying a second programming voltage to one of a plurality of bitlines corresponding to said cell to be programmed, wherein said second voltage gradually increases from a low level toward a high level;

c) monitoring a current on said one of said plurality of bitlines;

d) removing said first programming voltage when said current begins to decrease; and

e) removing said second programming voltage when said current begins to decrease.

7. The method according to Claim 6, wherein said memory device comprises a flash memory.

8. The method according to Claim 6, wherein said monitoring said current is adapted to reduce a distribution of said desired threshold voltage.

9. The method according to Claim 6, wherein said monitoring said current is adapted to increase a margin between said desired threshold voltage and an adjacent threshold voltage.

10. The method according to Claim 6, wherein said monitoring said current is adapted to increase a programming reliability of said memory cell.

11. A memory cell for storing a plurality of bits comprising:

a control gate, wherein one of a plurality of first programming voltages is applied until a drain current drops below a reference level;

a drain, wherein a ramped programming voltage is applied until said drain current drops below said reference level; and

a floating gate, wherein each of said plurality of first programming voltages causes a corresponding one of a plurality of levels of charge to be stored on said floating gate, and wherein each of said plurality of levels of charge represent one of a plurality of combinations of said plurality of bits.

12. The memory cell for storing a plurality of bits according to Claim 11, wherein said ramped programming voltage comprises a gradually increasing voltage.

13. The memory cell for storing a plurality of bits according to Claim 11, further comprising:

a source;

a channel disposed between said drain and said source; and

wherein said floating gate is disposed between said control gate and said channel.

14. The memory cell for storing a plurality of bits according to Claim 11, wherein said plurality of bits comprises two bits.

15. The memory cell for storing a plurality of bits according to Claim 14, wherein said plurality of levels of charge comprises four levels of charge.

16. The memory cell for storing a plurality of bits according to Claim 11, wherein said plurality of bits comprises three bits.

17. The memory cell for storing a plurality of bits according to Claim 16, wherein said plurality of levels of charge comprises eight levels of charge.

18. The memory cell for storing a plurality of bits according to Claim 11, wherein applying said ramped programming voltage until said drain current drops below said reference level is adapted to increase a programming reliability of said memory cell.

19. The memory cell for storing a plurality of bits according to Claim 11, wherein applying said ramped programming voltage until said drain current drops below said reference level is adapted to reduce a programming time.

20. The memory cell for storing a plurality of bits according to Claim 11, wherein applying said ramped programming voltage until said drain current drops below said reference level is adapted reduce a programming damage to said memory cell.